Claims

1-17 Canceled

18. (New) An analyzing device for an embedded system (9), comprising:

at least one CPU (1);

at least one CPU bus (2); and

at least one memory (3), including at least one communication module (4) for input or output of analysis data using a test interface (5), wherein the test interface, in addition to control lines, includes at least one group of data lines transmitting data words and address words alternately or in other succession, and information indicating whether data words or address words are transmitted is transmitted by way of at least one control line so that content and access operations during an operation time to a describable internal memory as well as I/O access operations of the embedded system can be monitored or logged practically without using basic cycles of the CPU (1)..

19. (New) A device according to claim 18, wherein there are two or more freely selectable analysis modes, with the analysis modes differing from each other in the way and extent of participation of the CPU 1 in reading or writing data for analysis purposes, and wherein depending on the selected analysis mode either all write access operations of the CPU to especially definable address ranges are logged without using basic cycles, or all read access operations of the CPU are logged, or direct reading and writing of the CPU from/into an external memory (6) is executed by using basic cycles.

20. (New) A device according to claim 18, wherein the communication module comprises a logic 22, 23 which independently has access to data or address information through a data connection in order to follow write or read access

operations in real time.

21 (New) A device according to claim 18, wherein the communication module is connected to a cache (8, 8', 8"), and data transmitted in write or read access operations can be stored in the cache, and data out of the cache can be output in a buffered manner through the test interface (5) or data can be written into the cache using the test interface, respectively.

22. (New) A device according to claim 18, wherein the test interface (5) is connected to a test memory (6) arranged outside the embedded system, and the external test memory (6) is especially a central core memory or a dual-port memory.

23. (New) A device according to claim 18, wherein the data transmission from the communication module to the external memory takes place through a parallel interface (5).

24. (New) A device according to claim 18, wherein the external memory (6) is connected to a data conditioning device (7) which provides an interface connection (14) for external debugging applications.

25. (New) A device according to claim 18, wherein the device is in an embedded system which comprises a fully operable microcomputer with at least central processing unit (1) and data memory (3).

26. (New) A device according to claim 18, wherein the device is in an integrated microprocessor system for motor vehicles with at least two processor cores (15, 16), wherein the device is associated with at least one of the processor cores (16) contained therein.

27. (New) A device according to claim 26, wherein that in addition to the first processor core (16) with the complete analyzing device, an incomplete analyzing device (17) is associated with another processor core (15) in the integrated microprocessor system, having a reduced scope of functions compared to the complete analyzing device (18).

28. (New) A device according to claim 27, wherein the reduction of the scope of functions involves that the cache (8' 8'') provided in the analyzing device has a small number of memory locations and/or a small word width, and/or the test interface (5) is not led to the outside, and/or the test interface (5) does not exist.

29. (New) A method for the analysis of an embedded system with a test interface, the method comprising:

in that for the transmission of data through the test interface, a data transmission protocol is used in which data is transmitted in several groups of addresses and data.

30. (New) A method according to claim 29, wherein at least one mode is provided in which analysis data in real time can be read out of the system which comprises at least CPU, data memory, program memory, and I/O element(s), or can be written into the system, so that the system need not be stopped or interrupted for the analysis.

31. (New) A method according to claim 30, wherein the memory content or a correspondingly assessable information of the embedded system is copied in real time completely or partly into an external memory, with the data being buffered in particular before the action, or the memory content of an external memory (6) or any correspondingly assessable information about the memory content of memory

(6) is copied in real time completely or partly into a memory of the embedded system, with the data being buffered in particular before the action.

32. (New) A method according to claim 29, wherein only data necessary for debugging is transmitted to the external memory (6) in the event of access operations of the CPU to RAM 3.

33. (New) A method according to claim 29, wherein write access operations or read access operations of the CPU are logged by means of a cache (8, 8', 8'').

34. (New) A method according to claim 33, wherein information about the write access operations are written into the cache (8, 8', 8'') without additional CPU commands or directly into a communication module (4), and information about the read access operations is written into the cache with active assistance of the CPU.